



Harsh Environment Applied Technologies INC

VideolR Camera Link Sensor

Interface Control Document

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1 INTRODUCTION

1.1 PURPOSE

The purpose of this document is to describe the interfaces of the LWIR Camera-Link Board with a level of detail that will allow a designer to understand the functional details of the interfaces. The Camera-Link board is a part of the LWIR Camera-Link Sensor. The LWIR Camera-Link board is a modification of the existing SCC500-X Camera Link board. The LWIR Camera-Link board supports the SCC500X/H/L and the MIM500X/H/L versions of the LWIR sensor.

1.2 REFERENCES

The following documents were used in preparing this specification:

1. LWIR CL-ICD, Rev 1.0
2. Camera Link LWIR Intfc Schematic, Rev 1.0
3. 500X-CL Schematic, Rev 1.6
4. BAE Systems MIM500 Electrical Interface Control Document A15652, Rev. 3, 7/13/2005.
5. BAE Systems SCC500 Electrical Interface Control Document 21101781, Rev. B, 7/1/2003.
6. BAE Systems SCC500X Electrical Interface Control Document 21102174, Rev. 1, 3/1/2004.
7. BAE Systems SCC500 Hardware Interface Control Document, Rev. 0.1, 9/24/02.
8. PULNiX America "Specifications of the Camera-Link Interface Standard for Digital Cameras and Frame Grabbers", October 2000.
9. Basler Vision Technologies "Camera-Link Technology Brief", Document DD-000601, Rev. 3/28/2001

1.3 DOCUMENT CONVENTIONS

The following sections describe conventions used in this document.

1.3.1 Terminology

The terms “input” and “output” are used throughout this document to specify the direction of data flow and are referenced with respect to the sensor, not the capturing device.

Multi-bit (n-bit) words are numbered with ‘n-1’ being the most significant bit and ‘0’ being the least significant bit. For example, BUS[9:0] refers to a 10-bit bus with the most significant bit in the BUS[9] position and the least significant bit in the BUS[0] position.

1.3.2 Units of Measure

All measurements and specifications in this document are based on the following units of measure, unless otherwise specified:

Table 1 – Units of Measure

| Measure | Unit |
|----------------|--|
| Voltage | Volts (V) |
| Current | Amperes (A) |
| Power | Watts (W) |
| Frequency | Hertz (Hz) |
| Time | Seconds (s) |
| Resistance | Ohms (Ω) |
| Capacitance | Farads (F) |
| Inductance | Henrys (H) |
| Temperature | Degrees Celsius ($^{\circ}\text{C}$) |
| Distance | Inches (“) |
| KiloByte | 1024 Bytes (KB) |

1.3.3 Acronyms

The following table defines the acronyms used throughout this document.

Table 2 - Acronyms

| Acronym | Definition |
|----------------|---|
| LWIR | Long Wave Infra-Red |
| CL | Camera-Link |
| ICD | Interface Control Document |
| FPA | Focal Plane Array |
| FPGA | Field Programmable Gate Array |
| 0x | The “0x” at the beginning of a number indicates hexadecimal format. |
| MBps | Megabytes per second |
| Mbps | Megabits per second |
| ppm | Parts Per Million |
| ms | Millisecond |
| ns | Nanosecond |
| us | Microsecond |
| I/O | Input / Output |
| R/W | Read/Write |
| FVAL | Frame Valid |
| LVAL | Line Valid |
| DVAL | Data Valid |
| FS | Frame Sync |
| LS | Line Sync |

2 OVERVIEW

The Long Wave Infra-Red (LWIR) Camera-Link sensor is a thermal camera that provides digital video output that conforms to the Camera-Link standard. The LWIR Camera Link sensor comes in two different flavors: SCC-500 and MIM-500. Each of these sensors has different versions based on the internal Focal Plane Array (FPA): “H/L” and “X”. The SCC-500 “H/L” sensor provides progressive (320x240) video at 60 frames per second. The SCC-500 “X” sensor provides progressive (640x480) video at 30 frames per second. The MIM-500 “X/H/L” sensors provide progressive (640x480) video at 60 frames per second. Both SCC-500 and MIM-500 sensors also provide an analog RS-170 video output. The following figure shows the external interfaces of the sensor for a typical application. The Camera-Link board is a part of the sensor, which provides the Camera-Link video interface to the user. The Camera-Link board receives a single LVDS video input from within the sensor and processes it into an output per the Camera-Link standard.

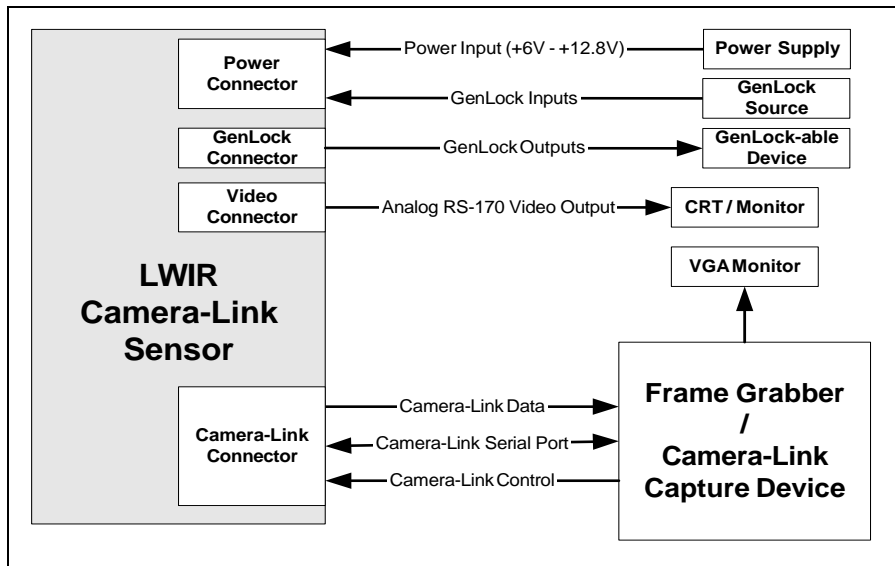


Figure 1 – LWIR Camera-Link Sensor Typical Application

3 ELECTRICAL INTERFACES

The following sections detail the electrical interfaces of the LWIR Camera-Link sensor.

3.1 CAMERA-LINK INTERFACE

The Camera-Link interface conforms to the Camera-Link standard. All Camera-Link signals are LVDS. The Camera-Link outputs from the sensor should be terminated into 100-ohm differential loads.

3.1.1 Serial Communication

The sensor implements the Camera-Link asynchronous serial communication using the SERTFG (camera to frame grabber) and the SERTC (frame grabber to camera) LVDS pairs. The serial protocol uses one start bit, one stop bit, no parity, and no handshaking with a baud rate of 115 Kbps or 38.4 Kbps. The baud rate setting is set at the factory.

The sensor powers up and initializes / configures itself to output Camera-Link. After the initial power-up, the serial port provides direct access to the SCC500 or MIM500 camera allowing the user to use the camera API commands.

Note that although all camera commands are available, the user should not modify the LVDS output mode or the camera baud rate using the serial port as this will lead to undesirable behavior. The LVDS output mode should be selected using the CC[2:1] signals. The baud rate is set at the factory.

3.1.2 Camera Controls

The LWIR Camera-Link sensor implements the four camera control signals (CC[4:1]) specified in the Camera-Link standard for controlling the camera with a frame grabber.

Camera Controls CC[2:1] are used to select the output mode of the sensor. These signals are level-sensitive as opposed to edge-triggered. The mapping of the output mode is shown in the following table.

Table 3 – Sensor Digital Video Output Mode Selection

| Camera Controls (CC[2:1]) | Output Mode | Pixel Data Width | Description | Notes |
|---------------------------|-------------|------------------|------------------------|-------|
| 00 | 0 | 14-bit pixel | Output from Up-sampler | |
| 01 | 1 | 10-bit pixel | Output from Equalizer | |
| 10 | 2 | 8-bit pixel | Output from Color LUT | |
| 11 | 3 | 8-bit pixel | Output from Overlay | |

Camera Control CC[3] is used to put the sensor in “freeze and hold” mode. In this mode, the sensor will continuously output the last frame. This control is edge-triggered. A low-to-high transition on CC[3] will put the sensor in the “freeze and hold” mode. A high-to-low transition on CC[3] will put the sensor back in normal operation.

Camera Control CC[4] is used to output a gray-scale test pattern. The size of the pixel (8/10/14-bits) is based on the output mode. A logic high on CC[4] enables the test pattern output.

3.1.3 Digital Video

The sensor outputs 8 to 14-bits of digital video (one pixel per cycle) based on the mode of operation as shown in the table. The digital video data and clocks are serialized 7-to-1 according to the Camera-Link standard using the Base Configuration and are made available on the Camera-Link connector in LVDS format. The following sub-sections outline the various versions of the LWIR sensor. The Camera-Link clock (XCLK) is 24.545MHz in all versions.

Note that the sensor requires time upon power-up in order to boot and configure itself. It is expected that the Camera-Link interface will be up ~10 seconds after power-up. FVAL and LVAL will be kept in inactive states during this initial power-up / boot / configuration time.

Table 4 – Camera-Link Output Based on Operation Mode

| Camera-Link Data bit | Mode 0 (Up-sampled) (CC[2:1] = 00) 14-bit pixel | Mode 1 (Equalized) (CC[2:1] = 01) 10-bit pixel | Mode 2 (Color LUT) (CC[2:1] = 10) 8-bit pixel | Mode 3 (Overlay) (CC[2:1] = 11) 8-bit pixel |
|----------------------|---|--|---|---|
| 27 (Port A6) | PixData[6] | PixData[6] | PixData[6] | PixData[6] |
| 26 (DVAL) | DVAL | DVAL | DVAL | DVAL |
| 25 (FVAL) | FVAL | FVAL | FVAL | FVAL |
| 24 (LVAL) | LVAL | LVAL | LVAL | LVAL |
| 23 (Spare) | Spare (not used) | Spare (not used) | Spare (not used) | Spare (not used) |
| 22 (Port C5) | - | - | - | - |
| 21 (Port C4) | - | - | - | - |
| 20 (Port C3) | - | - | - | - |
| 19 (Port C2) | - | - | - | - |
| 18 (Port C1) | - | - | - | - |
| 17 (Port C7) | - | - | - | - |
| 16 (Port C6) | - | - | - | - |
| 15 (Port C0) | - | - | - | - |
| 14 (Port B5) | PixData[13] (MSB) | - | - | - |
| 13 (Port B4) | PixData[12] | - | - | - |
| 12 (Port B3) | PixData[11] | - | - | - |
| 11 (Port B7) | - | - | - | - |
| 10 (Port B6) | - | - | - | - |
| 9 (Port B2) | PixData[10] | - | - | - |
| 8 (Port B1) | PixData[9] | PixData[9] (MSB) | - | - |
| 7 (Port B0) | PixData[8] | PixData[8] | - | - |
| 6 (Port A5) | PixData[5] | PixData[5] | PixData[5] | PixData[5] |
| 5 (Port A7) | PixData[7] | PixData[7] | PixData[7] (MSB) | PixData[7] (MSB) |
| 4 (Port A4) | PixData[4] | PixData[4] | PixData[4] | PixData[4] |
| 3 (Port A3) | PixData[3] | PixData[3] | PixData[3] | PixData[3] |
| 2 (Port A2) | PixData[2] | PixData[2] | PixData[2] | PixData[2] |
| 1 (Port A1) | PixData[1] | PixData[1] | PixData[1] | PixData[1] |
| 0 (Port A0) | PixData[0] (LSB) | PixData[0] (LSB) | PixData[0] (LSB) | PixData[0] (LSB) |

3.1.3.1 SCC500 “H/L” Sensor

The SCC500 “H/L” sensor has a 60Hz progressive 320x240 output. The frame format is shown in the following figure. As shown, during each Frame Sync (FVAL) interval, a total of 262.5 lines are

provided. Each line includes 390 pixels. During the first 240 lines, the first 320 pixels are valid and the last 70 pixels have no information. The last 22.5 lines of each frame sync interval do not include any valid pixels.

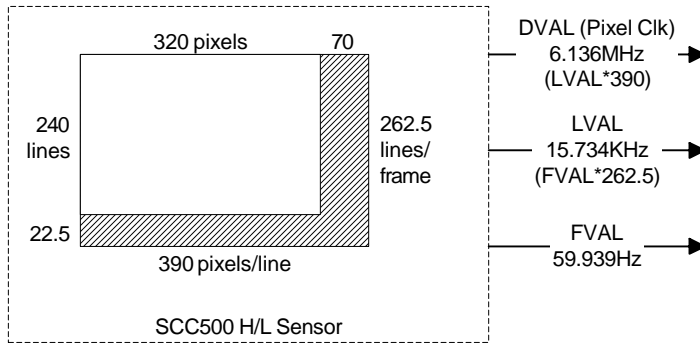


Figure 2 – SCC500H/L Sensor Frame Format

The Camera-Link clock (XCLK) is 24.545MHz corresponding to four times the pixel clock. The pixel clock (DVAL) is ~6.14MHz with one clock cycle per pixel. The pixel clock (DVAL) has a 25% duty cycle and is continuous (does not stop during blanking / invalid times).

The line valid (LVAL) is high (active) during active pixels. LVAL is low for 70 pixels (11.4us) during every line time (63.5us). The first pixel of valid video occurs on the first DVAL pulse following LVAL going active. There are 390 pixels per line, however only the first 320 pixels are valid.

The frame valid (FVAL) is high (active) during valid lines. FVAL is low for 22.5 lines (1.4ms) during every frame time (16.7ms). The first line of valid video occurs on the first LVAL pulse with FVAL active.

There is one pixel per DVAL cycle. The bit width of the pixel depends on the sensor mode selected using CC[2:1].

3.1.3.2 SCC500 “X” Sensor

The SCC500 “X” sensor has a 30Hz progressive 640x480 output. The frame format is shown in the following figure. As shown, during each Frame Sync (FVAL) interval, a total of 525 lines are provided. Each line includes 780 pixels. During the first 480 lines, the first 640 pixels are valid and the last 140 pixels have no information. The last 45 lines of each frame sync interval do not include any valid pixels.

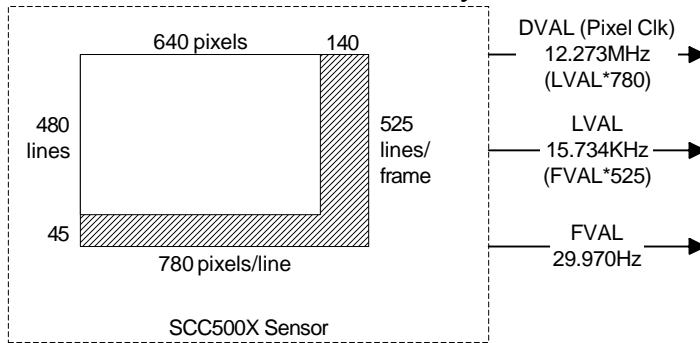


Figure 3 – SCC500X Sensor Frame Format

The Camera-Link clock (XCLK) is 24.545MHz corresponding to two times the pixel clock. The pixel clock (DVAL) is ~12.3MHz with one clock cycle per pixel. The pixel clock (DVAL) has a 50% duty cycle and is continuous (does not stop during blanking / invalid times).

The line valid (LVAL) is high (active) during active pixels. LVAL is low for 140 pixels (11.4us) during every line time (63.5us). The first pixel of valid video occurs on the first DVAL pulse following LVAL going active. There are 780 pixels per line, however only the first 640 pixels are valid.

The frame valid (FVAL) is high (active) during valid lines. FVAL is low for 45 lines (2.8ms) during every frame time (33.3ms). The first line of valid video occurs on the first LVAL pulse with FVAL active.

There is one pixel per DVAL cycle. The bit width of the pixel depends on the sensor mode selected using CC[2:1].

3.1.3.3 MIM500 “X/H/L” Sensor

The MIM500 “X/H/L” sensor has a 60Hz progressive 640x480 output. The frame format is shown in the following figure. As shown, during each Frame Sync (FVAL) interval, a total of 525 lines are provided. Each line includes 780 pixels. During the first 480 lines, the first 640 pixels are valid and the last 140 pixels have no information. The last 45 lines of each frame sync interval do not include any valid pixels.

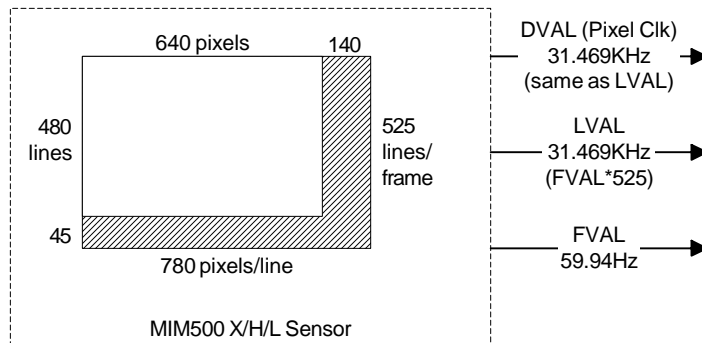


Figure 4 – MIM500 X/H/L Sensor Frame Format

The Camera-Link clock (XCLK) is 24.545MHz corresponding to the pixel clock. The pixel clock (DVAL) is identical to LVAL.

The line valid (LVAL) is high (active) during active pixels. LVAL is low for 140 pixels (5.7us) during every line time (31.8us). The first pixel of valid video occurs on the first XCLK pulse following LVAL going active. There are 780 pixels per line, however only the first 640 pixels are valid.

The frame valid (FVAL) is high (active) during valid lines. FVAL is low for 45 lines (1.4ms) during every frame time (16.7ms). The first line of valid video occurs on the first LVAL pulse with FVAL active.

There is one pixel per XCLK cycle. The bit width of the pixel depends on the sensor mode selected using CC[2:1].

3.2 ANALOG VIDEO OUTPUT

The LWIR Camera-Link Sensor has an analog RS-170 video output available on a SSMB connector. The RS-170 video output is 1Vp-p into a 75-ohm load.

3.3 POWER INPUT

The LWIR Camera-Link Sensor receives power from the power connector. The sensor accepts a range of +6VDC to +12.8VDC. The power supply should be capable of sourcing 2A.

3.4 MIM GEN-LOCKING

The MIM500 version of the LWIR Camera-Link Sensor is capable of gen-locking. The MIM version can output gen-lock signals (master mode) or receive gen-lock signals (slave mode). The configuration of master vs slave is through the serial port. Note that all gen-lock signals are LVDS.

A MIM500 gen-lock master outputs a nominal gen-lock clock of 12.2727MHz and a nominal gen-lock frame sync of 29.97Hz. The master gen-lock signals can be directly fed to a MIM500 gen-lock slave for locking the two sensors to one timing reference. Note that the gen-lock frame sync is actually $\frac{1}{2}$ the output frame rate.

If providing gen-lock signals externally, it is required that there are exactly 409,500 clock cycles per frame time. The gen-lock frame sync must be high for only one clock cycle in the frame. The gen-lock circuitry supports frequencies that are +/- 5% from the nominal 12.2727MHz clock leading to a frame rate range of 56.94Hz to 62.94Hz with a nominal frame rate of 59.94Hz.

By default, the MIM sensor runs in master mode and does not have the gen-lock circuitry enabled. In order to configure a MIM sensor to be a gen-lock master (and to output the gen-lock signals), the following commands should be sent via the serial port.

```
MIM:GLOC:ENAB ON  
CONF:GLOC:WAIT OFF
```

In order to configure a MIM sensor to be a gen-lock slave, the following commands should be sent via the serial port.

```
MIM:GLOC:ENAB ON  
CONF:GLOC:WAIT 10
```

After gen-lock commands are sent, the MIM sensor must be power-cycled for the commands to take effect.

4 MECHANICAL INTERFACES

The following sections describe the LWIR Camera-Link Sensor mechanical interfaces available via the connectors located on the back of the sensor enclosure. The orientation of the connectors on the back of the camera enclosure is shown in the figure below.

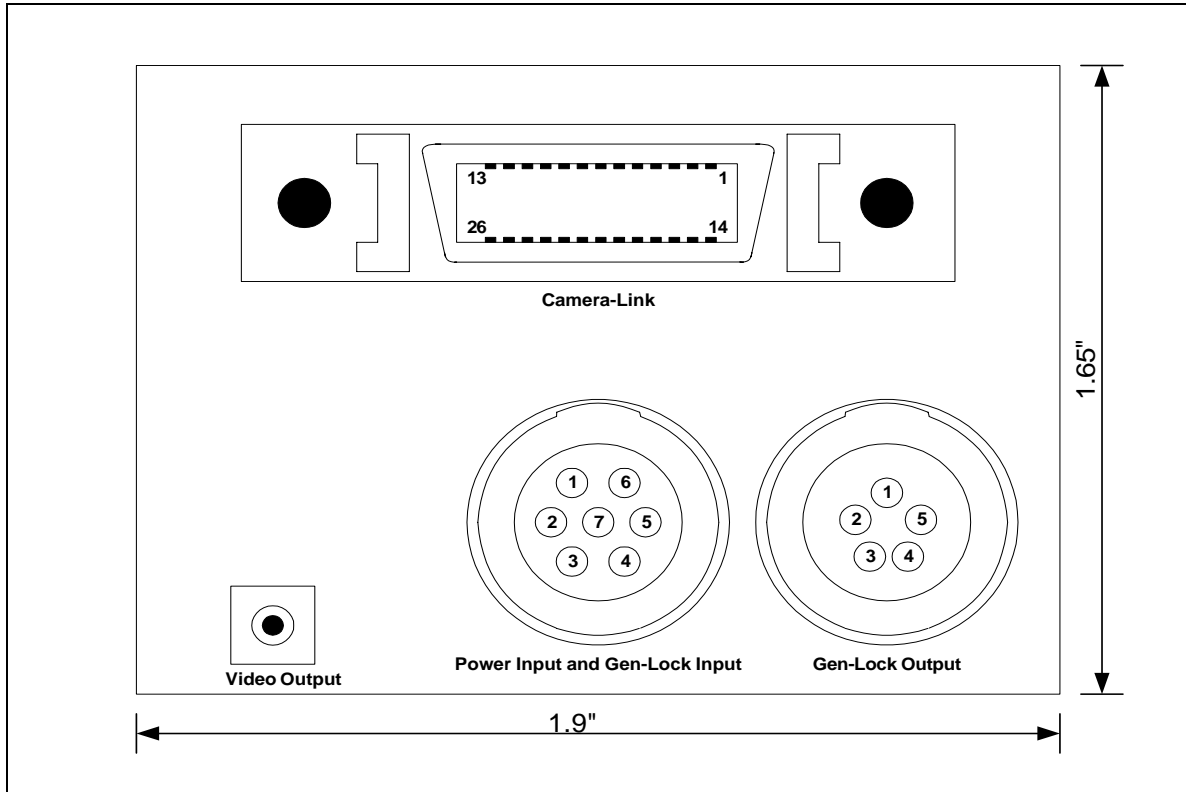


Figure 5 – LWIR Camera-Link Sensor Connector Orientation

4.1 POWER AND GEN-LOCK INPUT (TO CAMERA) CONNECTOR

A 7-pin connector (LEMO EEG.0B.307.C.L.N) is used for providing power to the sensor. The corresponding mating connector is LEMO FFG.0B.307.CLAD52. The connector is also used for providing the Gen-Lock input signals to the sensor. The following figure shows the connector pin-out.

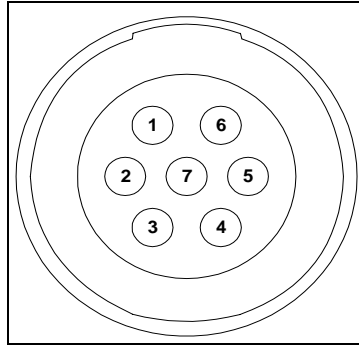


Figure 6 – Power / Gen-Lock Input Connector

Table 5 – Power / Gen-Lock Input Connector Pin-out

| Signal Name | Pin # | I/O | Note | Description |
|---------------|-------|-----|-------|--------------------------------------|
| VIN | 1 | I | Power | Power to sensor (+6V – +12.8V) |
| GND | 2 | P | Power | Ground |
| GENLOC-CLK-N | 3 | I | LVDS | Gen-Lock Clock (negative) input |
| GENLOC-CLK-P | 4 | I | LVDS | Gen-Lock Clock (positive) input |
| GENLOC-SYNC-P | 5 | I | LVDS | Gen-Lock Frame Sync (positive) input |
| GND | 6 | P | Power | Ground |
| GENLOC-SYNC-N | 7 | I | LVDS | Gen-Lock Frame Sync (negative) input |

4.2 GEN-LOCK OUTPUT (FROM CAMERA) CONNECTOR

A 5-pin connector (LEMO EEG.0B.305.C.L.N) is used for outputting the Gen-Lock signals from the sensor (for use by a slave). The corresponding mating connector is a LEMO FFG.0B.305.CLAD52. The following figure shows the connector pin-out.

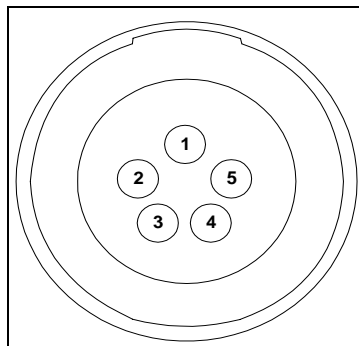


Figure 7 – Gen-Lock Output Connector

Table 6 – Gen-Lock Output Connector Pin-out

| Signal Name | Pin # | I/O | Note | Description |
|------------------|-------|-----|-------|---------------------------------------|
| GND | 1 | P | Power | Ground |
| GENLOC-CLKOUT-N | 2 | O | LVDS | Gen-Lock Clock (negative) output |
| GENLOC-CLKOUT-P | 3 | O | LVDS | Gen-Lock Clock (positive) output |
| GENLOC-SYNCOUT-N | 4 | O | LVDS | Gen-Lock Frame Sync (negative) output |
| GENLOC-SYNCOUT-P | 5 | O | LVDS | Gen-Lock Frame Sync (positive) output |

4.3 CAMERA-LINK CONNECTOR

A 26-pin connector (3M 10226-2200VE) is used for the Camera-Link interface. The corresponding mating connector is 3M 10126-3000VE. The connector pin-out conforms to the Camera-Link standard for a camera using the Base Configuration. The following shows the connector pin-out.

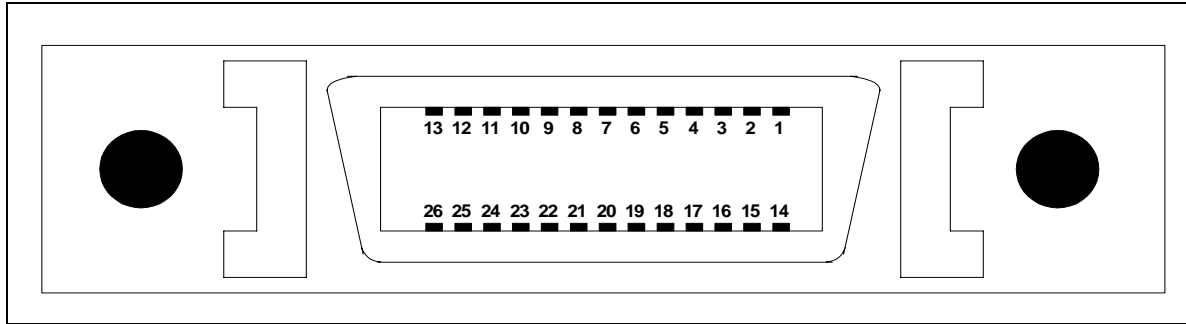


Figure 8 – Camera-Link Connector

Table 7 – Camera-Link Connector Pin-out

| Signal | Pin # | I/O | Note | Description |
|---------|-------|-----|------------|--|
| INSH | 1 | - | | Inner Shield |
| INSH | 14 | - | | Inner Shield |
| X0- | 2 | O | RS644/LVDS | Camera-Link Data Channel #0 (negative side) |
| X0+ | 15 | O | RS644/LVDS | Camera-Link Data Channel #0 (positive side) |
| X1- | 3 | O | RS644/LVDS | Camera-Link Data Channel #1 (negative side) |
| X1+ | 16 | O | RS644/LVDS | Camera-Link Data Channel #1 (positive side) |
| X2- | 4 | O | RS644/LVDS | Camera-Link Data Channel #2 (negative side) |
| X2+ | 17 | O | RS644/LVDS | Camera-Link Data Channel #2 (positive side) |
| XCLK- | 5 | O | RS644/LVDS | Camera-Link Clock Channel (negative side) |
| XCLK+ | 18 | O | RS644/LVDS | Camera-Link Clock Channel (positive side) |
| X3- | 6 | O | RS644/LVDS | Camera-Link Data Channel #3 (negative side) |
| X3+ | 19 | O | RS644/LVDS | Camera-Link Data Channel #3 (positive side) |
| SERTC+ | 7 | I | RS644/LVDS | Camera-Link Serial Communication Input (positive side) |
| SERTC- | 20 | I | RS644/LVDS | Camera-Link Serial Communication Input (negative side) |
| SERTFG- | 8 | O | RS644/LVDS | Camera-Link Serial Communication Output (negative side) |
| SERTFG+ | 21 | O | RS644/LVDS | Camera-Link Serial Communication Output (positive side) |
| CC1- | 9 | I | RS644/LVDS | Camera Control Channel #1 (negative side); used for mode sel |
| CC1+ | 22 | I | RS644/LVDS | Camera Control Channel #1 (positive side); used for mode sel |
| CC2+ | 10 | I | RS644/LVDS | Camera Control Channel #2 (positive side); used for mode sel |

| | | | | |
|------|----|---|------------|--|
| CC2- | 23 | I | RS644/LVDS | Camera Control Channel #2 (negative side); used for mode se |
| CC3- | 11 | I | RS644/LVDS | Camera Control Channel #3 (negative side); used for "freeze" |
| CC3+ | 24 | I | RS644/LVDS | Camera Control Channel #3 (positive side); used for "freeze" r |
| CC4+ | 12 | I | RS644/LVDS | Camera Control Channel #4 (positive side); used for test patte |
| CC4- | 25 | I | RS644/LVDS | Camera Control Channel #4 (negative side); used for test patt |
| INSH | 13 | - | | Inner Shield |
| INSH | 26 | - | | Inner Shield |

4.4 VIDEO OUTPUT CONNECTOR

A SSMB connector (Pasternack PE-4340) provides the analog RS-170 video output. The corresponding mating connector is Pasternack PE-4019. The following figure shows the connector.



Figure 9 – Video Output Connector